



BlackParrot

An Open Source RISC-V Multicore
For and By the World

<https://github.com/black-parrot>

U. Washington
Boston University

Presenter: Sadullah Canakci

BARC 2020



The BlackParrot "Genesis Release" Team



W

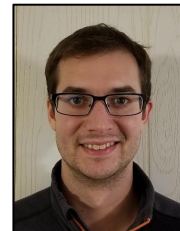
Prof. Michael Taylor



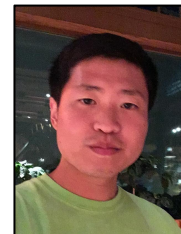
Dan Petrisko



Farzam Gilani



Mark Wyse

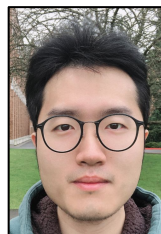


Tommy Jung



**BOSTON
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Prof. Ajay Joshi



Paul Gao



Sadullah Canakci



Zahra Azad



Scott Davidson



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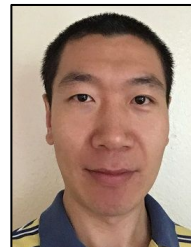
Prof. Mark Oskin



Yongqin Wang



Bandhav Veluri



Chun Zhao



Tavio Guarino

BlackParrot

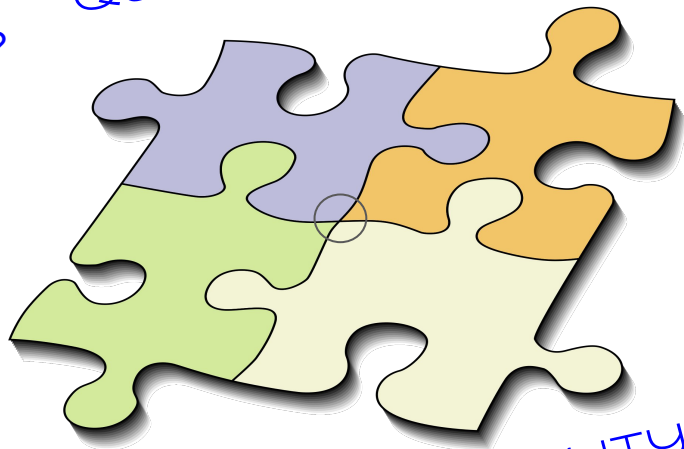
- It is an in-order 8-stage multi-core processor
- We implement the RISC-V “RV64G” architecture
- It supports three privilege levels (machine, supervisor, and user) as well as SV39 virtual memory
- We target running Linux (work in progress)
- It supports different accelerator interfaces (work in progress)
- We integrate BlackParrot into a Multi-FPGA board infrastructure (LiteX)

BlackParrot: Four Success Metrics

(achieve these and BlackParrot will become the Linux of RISC-V)

Will People Trust Our Code?
Is it easy to understand?
Is it secure?
Is it validated?

quality virality



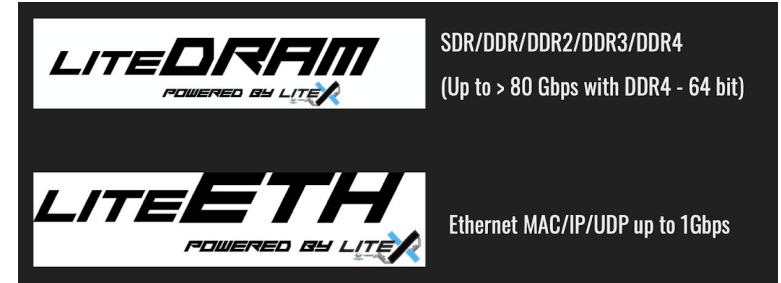
Scale to many users.
Get companies to invest and
become stewards of the code.

Is the code Pareto optimal in terms
of Power, Performance, and Area?

Does the code have the features
people need?
And leave out the ones they don't?

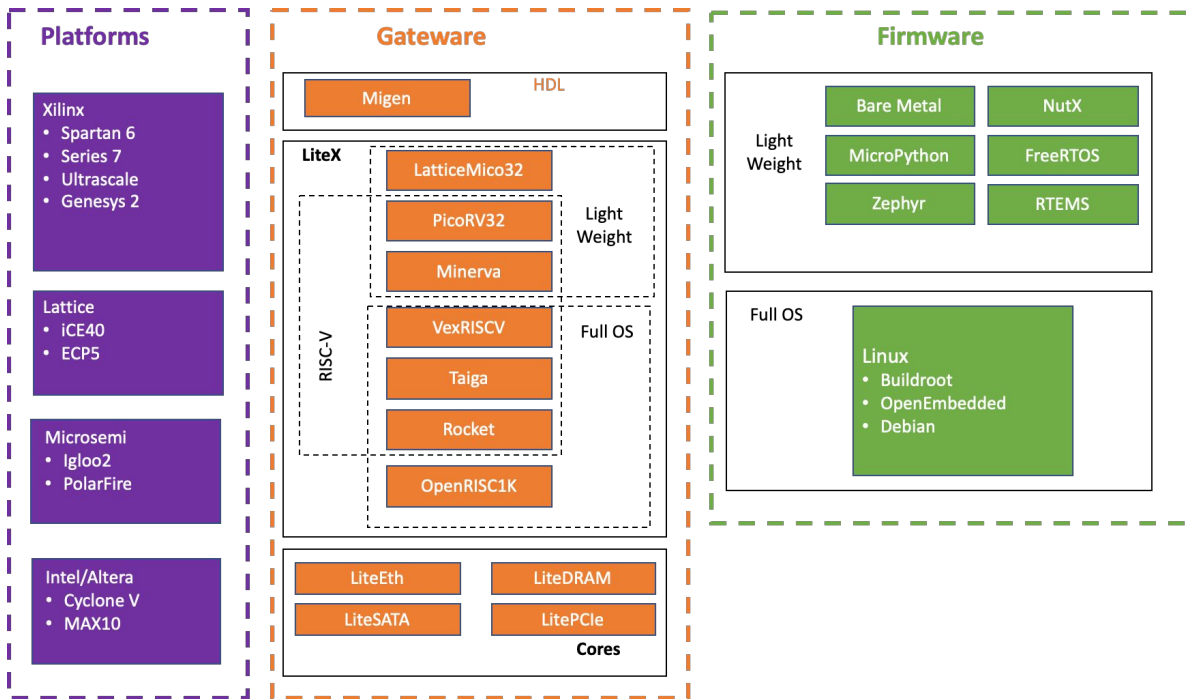
LiteX : Build your hardware, easily!

- LiteX is a python-based SoC builder that can be used to create SoCs and full FPGA designs [1].
- LiteX's Open Source Cores Ecosystem
 - LiteDRAM, LiteEth, LitePCIe, LiteSATA, LiteSDCard, LiteVideo



*Figures are retrieved from <https://osda.gitlab.io/19/1.1-slides.pdf>

LiteX : Build your hardware, easily!



Switch FPGA in command line:

```
./arty.py --cpu_type=Rocket
```

```
./genesys2.py --cpu_type=Rocket
```

Switch CPU in command line:

```
./arty.py --cpu_type=vexriscv
```

```
./arty.py --cpu_type=Rocket
```

Want to try it or to help :) ? :

<http://github.com/enjoy-digital/litex>

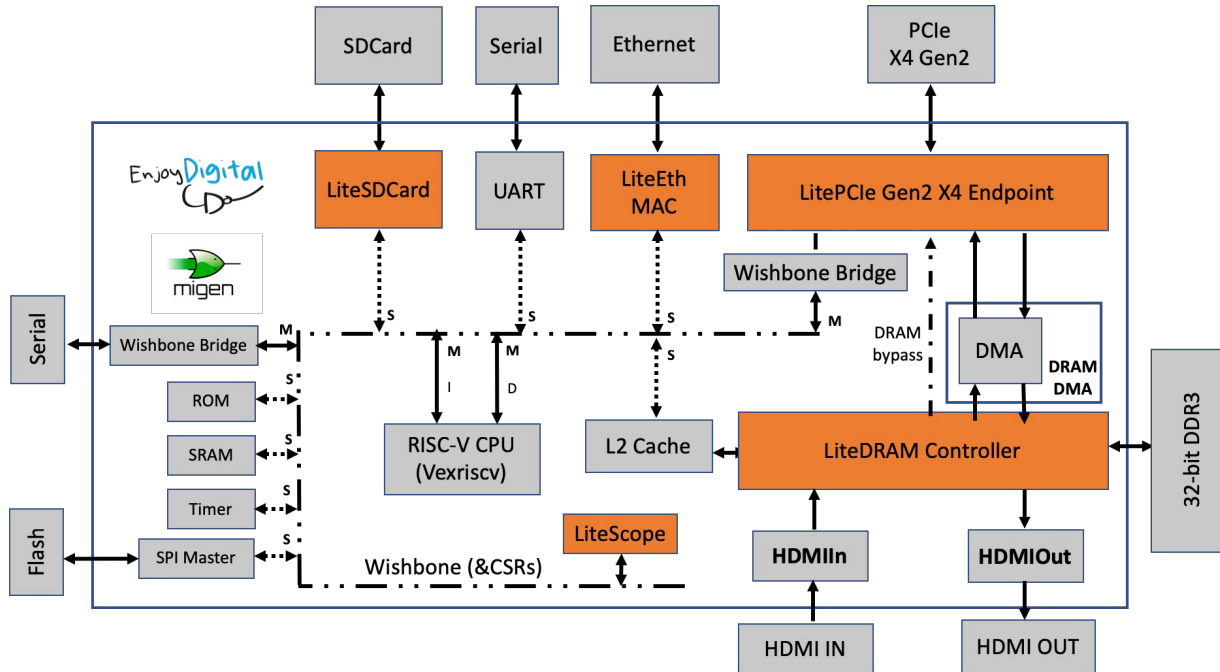
Get in touch on IRC (Freenode):

LiteX: #litex

*Figure is adapted by <https://github.com/timvideos/litex-buildenv/wiki>

Why BlackParrot in LiteX?

- Drive the adoption of BlackParrot by the FPGA enthusiast community by building support for BlackParrot into LiteX.



BlackParrot in LiteX - Current Status and Next Steps

- Current Status
 - *Simulated* (Verilator) BlackParrot in LiteX and successfully executed the "Litex BIOS".
 - Successfully run the "Litex BIOS" on the FPGA. We utilize UART interface of the FPGA to send and receive commands through keyboard.
- Next Steps
 - Integration of LiteEth which provides the capability of loading an user firmware into external memory via tftp.
 - Booting up Linux on FPGA.

```

  _____
 | 0 7 |
 | L I T E X |
 | _____ |

(c) Copyright 2012-2019 Enjoy-Digital
BIOS built on Dec 26 2019 16:11:17

Migen git sha1: 41922fd
LiteX git sha1: 6ald431

----- SoC -----
CPU:      BlackParrotRV64[ia] @ 1MHz
ROM:      64KB
SRAM:     4KB
L2:       8KB
MAIN-RAM: 65536KB

----- Initialization -----
Initializing SDRAM...
SDRAM now under hardware control
DEBUG memtest
Memtest OK

----- Boot -----
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
Timeout
No boot medium found

----- Console -----
litex> ident
Ident: LtXSmlto 091-61:11
litex> █
```


We need the “Linux of RISC-V Cores”

We want to gather a village...

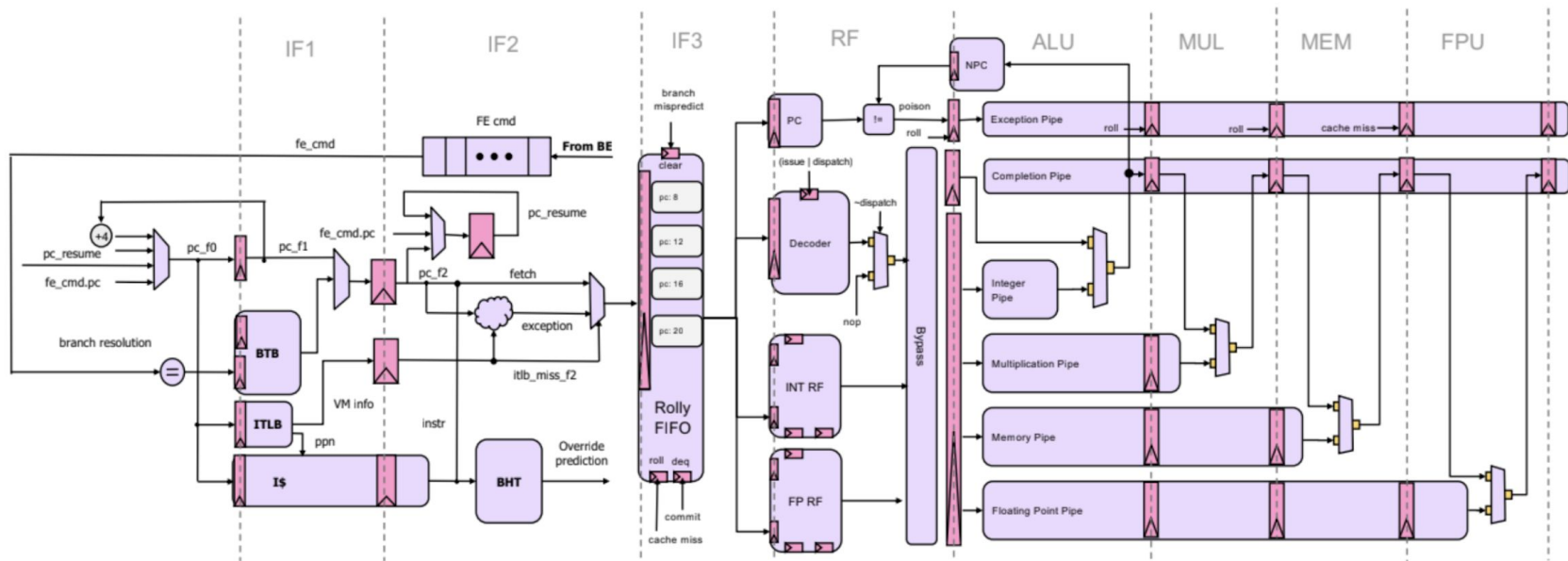
- to create free-and-open, reusable Pareto-optimal hardware
- to bring together highly specialized knowledge from all over the world
- to gather and incorporate feedback from industry and academic experts
- to crowdsource the best Linux-Capable 64-bit RISC-V multi-core



Pre-alpha version available at:
www.github.com/black-parrot

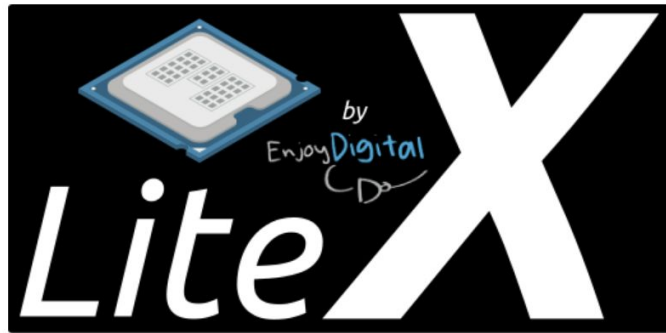
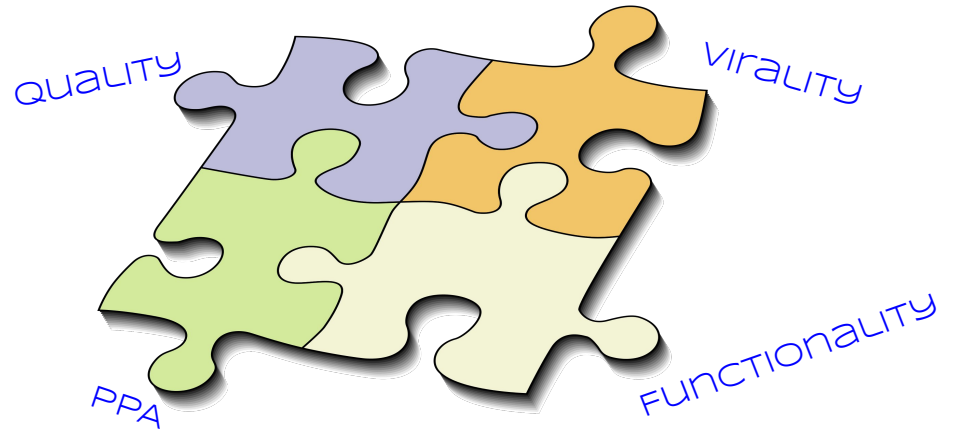
If you are interested in contributing,
come talk to me or email me at
scanakci@bu.edu

Backup Slides



Summary

<https://github.com/black-parrot>



Build your hardware, easily!

